What is claimed is:

1. A method of fabricating a semiconductor structure with partially etched gate, comprising the steps of:

providing a semiconductor substrate with at least two adjacent gate structures thereon, wherein each gate structure is composed of a gate dielectric layer, a gate conductive layer, a cap layer, sequentially stacked on the substrate, and a lining layer covered on sidewalls thereof;

sequentially forming a protective layer and a masking layer over the gate structures;

forming an opening in the masking layer and etching the protective layer thereunder to partially expose the lining layer covering one sidewall of the two adjacent gate structures;

removing the exposed lining layers;

removing the masking layer and the protective layer; and

forming a spacer overlying sidewalls of each gate structure to form a plurality of single-side partially etched gate structures.

2. The method as claimed in claim 1, further comprising, after removing the exposed lining layers, the step of partially removing the gate conductive layer adjacent to the exposed lining layer.

3. The method as claimed in claim 1, further comprising the steps of:

forming an inter-layer dielectric layer over the gate structures; and

performing photolithography and etching to form a bitline contact in the inter-layer dielectric layer and exposing the substrate and portions of the adjacent gate structures therein.

4. The method as claimed in claim 1, wherein the gate conductive layer is composed of a polysilicon layer and a metal silicide layer.

5. The method as claimed in claim 4, wherein material of the metal silicide layer is tungsten silicide.

6. The method as claimed in claim 1, wherein the protective layer is an anti-reflection coating (ARC) layer.

7. The method as claimed in claim 1, wherein material of the masking layer is photoresist (PR).

8. The method as claimed in claim 1, wherein materials of the cap layer and the spacer are silicon nitride.

9. The method as claimed in claim 1, wherein the lining layer is a rapid thermal oxide (RTO) layer.

10. The method as claimed in claim 4, wherein the gate structure adjacent to the exposed lining layer is the metal silicide layer.

11. The method as claimed in claim 3, wherein the opening is substantially relative to a position of the bitline contact.

12. The method as claimed in claim 3, wherein the method for forming the opening and the bitline contact is nanoimprint lithography (NIL) or photolithography.

13. The method as claimed in claim 1, wherein the reticle for forming the opening is bitline contact node reticle or bitline contact reticle.

14. The method as claimed in claim 1, wherein removal of the exposed lining layer is achieved using diluted hydrofluoric acid (DHF) or buffer of etching (BOE) etchant.

15. The method as claimed in claim 2, wherein partial removal of the gate conductive layer is achieved using of RCA1 etchant.

16. A semiconductor structure with a partially etched gate, comprising:

a semiconductor substrate;

a gate dielectric layer, a gate conductive layer and a cap layer, sequentially stacked on the substrate to form a gate structure; and

a lining layer disposed on sidewalls of the gate structure, wherein the lining layer disposed on one sidewall of the gate structure is partially etched to expose the adjacent gate structure.

17. The semiconductor structure as claimed in claim 16, further comprising:

an inter-layer dielectric layer covering the gate structure; and

a bitline contact formed in the inter-layer dielectric layer, exposing the substrate and a portion of the gate structure therein, wherein the lining layer of the exposed portion of the gate structure is partially removed.

18. The semiconductor structure as claimed in claim 16, wherein the exposed gate structure is the gate conductive layer.

19. The semiconductor structure as claimed in claim 18, wherein the gate conductive layer comprises a polysilicon layer and a metal silicide layer.

20. The semiconductor structure as claimed in claim 19, wherein the exposed gate structure is the metal silicide layer and portions thereof are partially etched.

21. The semiconductor structure as claimed in claim 16, further comprising a spacer disposed on sidewalls of each gate structure, covering the lining layer.

22. The semiconductor structure as claimed in claim 16, wherein the lining layer is a rapid thermal oxide (RTO) layer.

23. The semiconductor structure as claimed in claim 21, wherein material of the spacer is silicon nitride.

24. A method of fabricating a semiconductor structure with partially etched gate, comprising the steps of:

providing a semiconductor substrate with at least two adjacent gate structures thereon, wherein each gate structure is composed of a gate dielectric layer, a gate conductive layer, a cap layer, sequentially stacked on the substrate, and a lining layer covered on sidewalls thereof;

forming a protective layer over the gate structures;

etching portions of the protective layer to partially expose the lining layer covering two sidewalls of each gate structure;

removing the exposed lining layers;

removing the protective layer; and

forming a spacer overlying sidewalls of each gate structures to form a plurality of dual-sided partially etched gate structure.

25. The method as claimed in claim 24, further comprising, before removing the partially exposed lining layers, the steps of:

forming a masking layer over the protective layer; and

forming a plurality of masking patterns in the masking layer, respectively covering the protective layer over the gate structures.

26. The method as claimed in claim 24, further comprising, after removing the exposed lining layers, the step of partially removing the gate conductive layer adjacent to the exposed lining layers.

27. The method as claimed in claim 24, further comprising the steps of:

forming an inter-layer dielectric (ILD) layer over the gate structures; and

performing photolithography and etching to form a bitline contact in the inter-layer dielectric layer and exposing the substrate and portions of the adjacent gate structures therein.

28. The method as claimed in claim 24, wherein the gate conductive layer is composed of a polysilicon layer and a metal silicide layer.

29. The method as claimed in claim 24, wherein materials of the protective layer are an anti-reflection coating (ARC) and photoresist (PR).

30. The method as claimed in claim 24, wherein the protective layer is an anti-reflection coating (ARC) layer and the masking layer is a photoresist (PR) layer.

31. The method as claimed in claim 24, wherein materials of the cap layer and the spacer are silicon nitride.

32. The method as claimed in claim 27, wherein the gate structure adjacent to the exposed lining layer is the metal silicide layer.

33. The method as claimed in claim 24, wherein removal of the exposed lining layer is achieved using diluted hydrofluoric acid (DHF) or buffer of etching (BOE) etchant.

34. The method as claimed in claim 26, wherein partially removing the gate conductive layer is achieved using RCA1 solution containing ammonium hydroxide (NH_4OH) and hydrogen peroxide (H_2O_2).

35. A semiconductor structure with a partially etched gate, comprising:

a semiconductor substrate;

a gate dielectric layer, a gate conductive layer and a cap layer, sequentially stacked on the substrate to form a gate structure; and

a lining layer disposed on sidewalls of the gate structure, wherein the lining layer disposed on two sidewalls of the gate structure is partially etched to expose the adjacent gate structure.

36. The semiconductor structure as claimed in claim 35, further comprising:

an inter-layer dielectric layer covering the gate structure; and

a contact formed in the inter-layer dielectric layer, exposing the substrate and a portion of the gate structure therein, wherein the lining layer of the exposed portion of the gate structure is partially removed.

37. The semiconductor structure as claimed in claim 35, wherein the exposed gate structure is the gate conductive layer.

38. The semiconductor structure as claimed in claim 37, wherein the gate conductive layer comprises a polysilicon layer and a silicide layer.

39. The semiconductor structure as claimed in claim 38, wherein the exposed gate structure is the metal silicide layer with partially etched portions.

40. The semiconductor structure as claimed in claim 35, further comprising a spacer disposed on sidewalls of the gate structure, covering the lining layer.

41. The semiconductor structure as claimed in claim 35, wherein the lining layer is a rapid thermal oxide (RTO) layer.

42. The semiconductor structure as claimed in claim 40, wherein material of the spacer is silicon nitride.